

## REMARKS

Claims 1-25 are pending in the application. The Examiner's reconsideration of the rejections in view of the amendments and remarks is respectfully requested.

Claims 1-24 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Chauvel et al. (U.S. Patent No. 6,369,855) in view of Sussman et al. (U.S. Patent No. 5,686,960). The Examiner stated essentially that the combined teachings of Chauvel and Sussman teach or suggest all the limitations recited in Claims 1-24.

Claims 1, 5, 9, and 17 are the independent claims.

Claims 1, 5, 9, and 17 claim, *inter alia*, “an X-data cache for storing a first data group managed by the coprocessor; and a Y-data cache for storing a second data group managed by the coprocessor.”

Chauvel teaches an audio-visual circuit (see Abstract). Chauvel fails to teach or suggest “an X-data cache for storing a first data group managed by the coprocessor; and a Y-data cache for storing a second data group managed by the coprocessor” as claimed in Claims 1, 5, 9, and 17. Chauvel teaches that the Communications Co-Processor “module 280 contains a collection of buffers, control registers, and control logic for various interfaces, such as UARTs, IR/RF, I.sup.2 C, and JTAG. All the buffers and registers are memory mapped and individually managed by the ARM CPU 220” (see col. 56, lines 56-60). Chauvel’s system manages data using the ARM CPU. Chauvel fails to teach or suggest cache managed by a co-processor, essentially as claimed in Claims 1, 5, 9, and 17.

Sussman teaches an image input device (see Abstract). Sussman fails to teach or suggest “an X-data cache for storing a first data group managed by the coprocessor; and a Y-data cache for storing a second data group managed by the coprocessor” as claimed in Claims 1, 5, 9, and

17. Sussman teaches a dedicated image processor (see col. 6, lines 36-38). The image processor of Sussman controls an X cache and a Y cache. Sussman does not teach or suggest a X-data cache not Y-data cache for storing data managed by a coprocessor. Further, nowhere does Sussman teach that the image processor manages data of another processor – the image processor is not analogous to a co-processor as claimed in Claims 1, 5, 9, and 17. Therefore, Sussman fails to cure the deficiencies of Chauvel.

The combined teachings of Chauvel and Sussman teach memory managed by a processor. The combined teachings of Chauvel and Sussman fail to teach or suggest a coprocessor, much less “an X-data cache for storing a first data group managed by the coprocessor; and a Y-data cache for storing a second data group managed by the coprocessor” as claimed in Claims 1, 5, 9, and 17.

Claims 2-4 depend from Claim 1. Claims 6-8 depend from Claim 5. Claims 10-16 depend from Claim 9. Claims 18-24 depend from Claim 17. The dependent claims are believed to be allowable for at least the reasons given for the respective independent claims.

At least Claim 21 is believed to be allowable for additional reasons.

Claim 21 claims, *inter alia*, “wherein the X-data field and the Y-data field overlap, and wherein an area of overlap is the microprocessor data field.”

Chauvel teaches an audio-visual circuit (see Abstract). Chauvel fails to teach or suggest “the X-data field and the Y-data field overlap, and wherein an area of overlap is the microprocessor data field” as claimed in Claim 21. Chauvel teaches an external memory (see col. 11, line 45). Chauvel fails to teach or suggest that an X-data field and a Y-data field overlap, and an area of overlap is a microprocessor data field, essentially as claimed in Claim 21.

Sussman teaches an image input device (see Abstract). Sussman fails to teach or suggest “the X-data field and the Y-data field overlap, and wherein an area of overlap is the microprocessor data field” as claimed in Claim 21. Sussman teaches an X cache and a Y cache (see col. 33, lines 28-34). Sussman’s X cache and Y cache are separate memory devices (see Figure 30). Sussman does not teach or suggest that an X-data field and a Y-data field overlap, much less that an area of overlap is the microprocessor data field, essentially as claimed in Claim 21. Therefore, Sussman fails cure the deficiencies of Chauvel.

Chauvel and Sussman, taken in combination or individually, fail to teach or suggest “the X-data field and the Y-data field overlap, and wherein an area of overlap is the microprocessor data field,” as claimed in Claim 21.

Therefore, Claim 21 is believed to be in condition for allowance.

The Examiner’s reconsideration of the rejection is respectfully requested.

New Claim 25 depends from Claim 5. Claim 25 is believed to be allowable for at least the reasons given for Claim 5. Claim 25 is believed to be allowable for additional reasons.

Claim 25 claims, “an external memory segmented into an X-data field for storing data of the X-data cache, a Y-data field for storing data of the Y-data cache, and a microprocessor data field, wherein the X-data field and the Y-data field overlap, and wherein an area of overlap is the microprocessor data field.”

Similar to Claim 21, Chauvel and Sussman, taken in combination or individual, fail to teach or suggest “an external memory segmented into an X-data field for storing data of the X-data cache, a Y-data field for storing data of the Y-data cache, and a microprocessor data field, wherein the X-data field and the Y-data field overlap, and wherein an area of overlap is the microprocessor data field,” as claimed in Claim 25.

Therefore, Claim 25 is believed to be in condition for allowance.

For the forgoing reasons, the application, including Claims 1-25, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

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